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1 **Fanin ordering in multi-shot timing analysis**
van Ginneken, L.P.P.P.;
Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceedings., IEEE 1992 International Conference on , 11-14 Oct. 1992
Pages:44 - 47

[Abstract] [PDF Full-Text (284 KB)] **IEEE CNF**

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Published before January 2001
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Relevance scale

1 Speeding up technology-independent timing optimization by network partitioning
Rajat Aggarwal, Rajeev Murgai, Masahiro Fujita
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(189.22 KB) Publisher Site
Additional Information: full citation, abstract, references, index terms

Technology-independent timing optimization is an important problem in logic synthesis. Although many promising techniques have been proposed in the past, unfortunately they are quite slow and thus impractical for large networks. In this paper, we propose DEPART, a delay-based partitioner-cum-optimizer, which purports to solve this problem. Given a combinational logic network that is to be optimized for timing, DEPART divides it into sub-networks using timing information and a constraint on the m ...

2 Concurrent logic restructuring and placement for timing closure
Jinan Lou, Wei Chen, Massoud Pedram
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(124.02 KB)
Additional Information: full citation, abstract, references, citings, index terms

In this paper, an algorithm for simultaneous logic restructuring and placement is presented. This algorithm first constructs a set of super-cells along the critical paths and then generates the set of non-inferior re-mapping solutions for each supercell. The best mapping and placement solutions for all super-cells are obtained by solving a generalized geometric programming (GGP) problem. The process of identifying and optimizing the critical paths is iterated until timing closure is achieve ...

3 A heuristic algorithm for the fanout problem
Kanwar Jit Singh, Alberto Sangiovanni-Vincentelli
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**
Full text available: pdf(651.94 KB)
Additional Information: full citation, abstract, references, citings, index terms

We present an algorithm to optimally distribute a signal to its required destinations. The choice of the buffers and the topology of the distribution tree depends on the availability of different strength gates and on the load and the required times at the destinations. The general problem is to construct a fanout-tree for a signal so that the required time constraint at the source node is met and the fanout-tree has a minimum area. Since the

area constrained fanout problem is NP-complete a ...

4 Query evaluation techniques for large databases

Goetz Graefe

June 1993 **ACM Computing Surveys (CSUR)**, Volume 25 Issue 2

Full text available: pdf(9.37 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Database management systems will continue to manage large data volumes. Thus, efficient algorithms for accessing and manipulating large sets and sequences will be required to provide acceptable performance. The advent of object-oriented and extensible database systems will not solve this problem. On the contrary, modern data models exacerbate the problem: In order to manipulate large sets of complex objects as efficiently as today's database systems manipulate simple records, query-processi ...

Keywords: complex query evaluation plans, dynamic query evaluation plans, extensible database systems, iterators, object-oriented database systems, operator model of parallelization, parallel algorithms, relational database systems, set-matching algorithms, sort-hash duality

5 Session 8C: advances in layout and synthesis: Layout-driven area-constrained timing optimization by net buffering

Rajeev Murgai

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(252.73 KB) Additional Information: full citation, abstract, references

With the advent of deep sub-micron technologies, interconnect loads and delays are becoming significant, and layout-driven synthesis has become the need of the day. However, given the tight constraints imposed by the layout (e.g., area availability, congestion), only those synthesis transforms can be made layout-driven that are local and layout-friendly. Examples of such transforms are net buffering, gate resizing, and gate replication.In this paper, we address the problem of minimizing the dela ...

6 LATTIS: an iterative speedup heuristic for mapped logic

J. P. Fishburn

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(494.10 KB) Additional Information: full citation, references, citings, index terms

7 Telescopic units: increasing the average throughput of pipelined designs by adaptive latency control

Luca Benini, Enrico Macii, Massimo Poncino

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(230.63 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a technique, alternative to performance-drivensynthesis, that allows to drastically increase the averagethroughput of combinational logic blocks by transforming fixed-latencyunits into variable-latency ones that run with a fasterclock cycle.The transformation is fully automatic and can beused in conjunction with traditional design techniques, such aspipelining, to improve the overall performance of speed-criticalsystems.Results, obtained on a large set of benchmark circuits,a ...

8 Timing optimization on mapped circuits

Ko Yoshikawa, Hiroshi Ichiryu, Hisato Tanishita, Sigenobu Suzuki, Nobuyoshi Nomizu, Akira Kondoh
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(597.35 KB) Additional Information: full citation, references, citings, index terms

9 Exact required time analysis via false path detection
Yuji Kukimoto, Robert K. Brayton
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(133.77 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper addresses how to compute required times at intermediatenodes in a combinational network given required times atprimary outputs. The simplest approach is to compute them basedon topological delay analysis without any consideration of falsepaths. In this paper, however, we take into account false pathsbetween the intermediate nodes and the primary outputs explicitlyto characterize the timing constraints at the nodes more accurately.We show that this approach leads to a technique for com ...

10 A depth-decreasing heuristic for combinational logic: or how to convert a ripple-carry adder into a carry-lookahead adder or anything in-between
John P. Fishburn
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(508.69 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a heuristic for speeding up combinational logic by decreasing the logic depth, at the expense of a minimal increase in circuit size. The heuristic iteratively speeds up sections of the critical path by the use of Shannon factorization on the late input. This procedure is empirically found to be capable of reproducing or even beating several classic global optimizations: a chain of an associative operator is transformed into a tree, a ripple prefix circuit into a paralle ...

11 Power minimization in IC design: principles and applications
Massoud Pedram
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

12 Retiming-based factorization for sequential logic optimization
Surendra Bommu, Niall O'Neill, Maciej Ciesielski

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Full text available: pdf(193.60 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Current sequential optimization techniques apply a variety of logic transformations that mainly target the combinational logic component of the circuit. Retiming is typically applied as a postprocessing step to the gate-level implementation obtained after technology mapping. This paper introduces a new sequential logic transformation which integrates retiming with logic transformations at the technology-independent level. This transformation is based on implicit retiming across logic blocks ...

Keywords: finite stat machines, retiming, sequential synthesis

13 Transistor reordering for power minimization under delay constraint

S. C. Prasad, K. Roy

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Full text available: pdf(289.98 KB) Additional Information: full citation, abstract, references, citings, index terms

In this article we address the problem of optimization of VLSI circuits to minimize power consumption while meeting performance goals. We present a method of estimating power consumption of a basic or complex CMOS gate which takes the internal capacitances of the gate into account. This method is used to select an ordering of series-connected transistors found in CMOS gates to achieve lower power consumption. The method is very efficient when used by library-based design styles. We describe ...

Keywords: circuit optimization, critical path enumeration, gate input reordering, power estimation, transistor reordering

14 Fast post-placement rewiring using easily detectable functional symmetries

Chih-Wei Chang, Chung-Kuan Cheng, Peter Suaris, Malgorzata Marek-Sadowska

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(59.40 KB) Additional Information: full citation, abstract, references, citings, index terms

Timing convergence problem arises when the estimations made during logic synthesis can not be met during physical design. In this paper, an efficient rewiring engine is proposed to explore maximal freedom after placement. The most important feature of this approach is that the existing placement solution is left intact throughout the optimization. A linear time algorithm is proposed to detect functional symmetries in the Boolean network and is used as the basis for rewiring. Integration wit ...

15 Performance optimization of sequential circuits by eliminating retiming bottlenecks

Sujit Dey, Miodrag Potkonjak, Steven G. Rothweiler

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(696.96 KB) Additional Information: full citation, references, citings, index terms

16 Performance optimization using separator sets

Yutaka Tamiya

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(104.95 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we propose a new method to optimize a performance of a very large circuit.

We find the best set of local transformations to be applied to the circuit, by inserting "padding nodes" on non-critical edges of the circuit, and calculating separator sets of the circuit using separator sets. Our method is robust for very large circuits, because its memory usage and calculation time are linear and polynomial order with the size of the circuit.According to our e ...

17 Area and delay mapping for table-look-up based field programmable gate arrays
P. Sawkar, D. Thomas
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Full text available: pdf(571.21 KB) Additional Information: full citation, references, citings, index terms

18 Optimization of critical paths in circuits with level-sensitive latches
Timothy M. Burks, Karem A. Sakallah
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(652.85 KB) Additional Information: full citation, abstract, references, index terms

A simple extension of the critical path method is presented which allows more accurate optimization of circuits with level-sensitive latches. The extended formulation provides a sufficient set of constraints to ensure that, when all slacks are non-negative, the corresponding circuit will be free of late signal timing problems. Cycle stealing is directly permitted by the formulation. However, moderate restrictions may be necessary to ensure that the timing constraint graph is acyclic. Forcin ...

19 Transformational placement and synthesis
Wilm Donath, Prabhakar Kudva, Leon Stok, Lakshmi Reddy, Andrew Sullivan, Kanad Chakraborty, Paul Villarrubia
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(79.97 KB) Additional Information: full citation, references, citings, index terms
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20 A methodology and algorithms for post-placement delay optimization
Lalgudi N. Kannan, Peter R. Suaris, Hong-Gee Fang
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(286.26 KB) Additional Information: full citation, references, citings, index terms

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Relevance scale

21 Low power synthesis of dual threshold voltage CMOS VLSI circuits
Vijay Sundararajan, Keshab K. Parhi
August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**
Full text available: pdf(751.10 KB) Additional Information: full citation, references, citings, index terms

22 Wireplanning in logic synthesis
Wilsin Gosti, Amit Narayan, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(938.17 KB) Additional Information: full citation, references, citings, index terms

23 A DSM design flow: putting floorplanning, technology-mapping, and gate-placement together
Amir H. Salek, Jinan Lou, Massoud Pedram
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(446.23 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents an integrated design flowwhich combines floorplanning, technology mapping, andplacement using a dynamic programming algorithm. Theproposed design flow consists of five steps: maximum treesub-structure formation, levelized cluster tree construction,minimum area implementation using 2-D shape functions,critical path identification, and repeated application ofsimultaneous floorplanning, technology mapping and gateplacement along the timing critical paths. Experimentalresults obt ...

24 On area/depth trade-off in LUT-based FPGA technology mapping
Jason Cong, Yuzheng Ding
July 1993 **Proceedings of the 30th international conference on Design automation**
Full text available: pdf(799.00 KB) Additional Information: full citation, references, citings, index terms

25

An exact algorithm for low power library-specific gate re-sizing
De-Sheng Chen, Majid Sarrafzadeh
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(650.44 KB) Additional Information: full citation, references, citings, index terms

26 Generalized matching from theory to application
Patrick Vuillod, Luca Benini, Giovanni De Micheli
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(252.57 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

We present a novel approach for post-mapping optimization. We exploit the concept of generalised matching, a technique that finds symbolically all possible matching assignments of library cells to a multi-output network specified by a Boolean relation. Several objectives are targeted: area minimization under delay constraints; power minimization under delay constraints; and unconstrained delay minimization. We describe the theory of generalized matching and the algorithmic optimization required ...

Keywords: Boolean relation, MCNC 91 benchmark suite, algorithmic optimization, area minimization, delay constraints, generalized matching, library cells, logic CAD, multi-output network, post-mapping optimization, power minimization, unconstrained delay minimization

27 Retiming for DSM with area-delay trade-offs and delay constraints
Abdallah Tabbara, Robert K. Brayton, A. Richard Newton
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(82.16 KB) Additional Information: full citation, references, citings, index terms

28 Removing user specified false paths from timing graphs
David Blaauw, Rajendran Panda, Abhijit Das
June 2000 **Proceedings of the 37th conference on Design automation**
Full text available: pdf(78.21 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a new method for removing user-specified false subgraphs from timing analysis and circuit optimization. Given a timing graph and a list of specified false paths, false subpaths, or false subgraphs, we generate a new timing graph in which all specified false paths are removed using a process of node splitting and edge removal. We present the necessary and sufficient condition for splitting a node, and show that the number of nodes that must be added to the timing graph is ...

29 On average power dissipation and random pattern testability of CMOS combinational logic networks
Amelia Shen, Abhijit Ghosh, Srinivas Devadas, Kurt Keutzer
November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(778.90 KB) Additional Information: full citation, references, citings, index terms

30 A gate resizing technique for high reduction in power consumption
P. Girard, C. Landrault, S. Pravossoudovitch, D. Severac
August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

Full text available: pdf(864.28 KB) Additional Information: full citation, references, citings

31 A simple algorithm for fanout optimization using high-performance buffer libraries
K. Kodandapani, J. Grodstein, A. Domic, H. Touati
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(525.37 KB) Additional Information: full citation, references, citings

32 Meeting delay constraints in DSM by minimal repeater insertion
I-Min Liu, Adnan Aziz, D. F. Wong
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(237.16 KB) Publisher Site Additional Information: full citation, references, index terms

33 A survey of optimization techniques targeting low power VLSI circuits
Srinivas Devadas, Sharad Malik
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**
Full text available: pdf(92.05 KB) Additional Information: full citation, references, citings, index terms

Keywords: low power, optimization, synthesis

34 Boolean techniques for low power driven re-synthesis
R. Iris Bahar, Fabio Somenzi
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(256.46 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We present a boolean technique to reduce power consumption of combinational circuits that have already been optimized for area and delay and then mapped onto a library of gates. In order to achieve a better optimization, we cluster gates by collapsing two or more levels of gates into a single node. When optimizing each cluster, our method extends the algorithms used in ESPRESSO, by adding heuristics that bias the minimization toward lowering the power dissipation in the circuit. The results of o ...

35 Integrated resynthesis for low power
Olivier Coudert, Ramsey Haddad
August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**
Full text available: pdf(241.06 KB) Additional Information: full citation, references, citings, index terms

36 Data security for Web-based CAD
Scott Hauck, Stephen Knol
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(198.79 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Internet-based computing has significant potential for improving most high-performance computing, including VLSI CAD. In this paper we consider the ramifications of the Internet on electronics design, and develop two models for Web-based CAD. We also investigate the security of these systems, and propose methods for protection against threats both from unrelated users, as well as from the CAD tools and tool developers themselves. These techniques provide methods for hiding unnecessary infor ...

Keywords: Internet, Web-based CAD, data security, encryption

37 Variable voltage scheduling
Salil Raje, Majid Sarrafzadeh
April 1995 **Proceedings of the 1995 international symposium on Low power design**
Full text available: pdf(205.51 KB) Additional Information: full citation, references, citings, index terms

38 The practical application of retiming to the design of high-performance systems
Brian Lockyear, Carl Ebeling
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(892.07 KB) Additional Information: full citation, references, citings

39 A fast fanout optimization algorithm for near-continuous buffer libraries
David S. Kung
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(186.04 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a gain-based fanout optimization algorithm for near-continuous buffer libraries. A near-continuous buffer library contains many buffers in a wide range of discrete sizes and each buffer of a specific type satisfies a size-independent delay equation. The new fanout algorithm is derived from an optimal algorithm to a special fanout optimization problem for continuous libraries. The gain-based technique constructs fanout trees which have better timing at similar area cost. ...

Keywords: fanout optimization, gate-sizing, logic synthesis

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